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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,631	07/24/2003	Noriyuki Ito	122.1444D	8072

21171 7590 08/08/2006

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EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,631	ITO ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14,15,28 and 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14,15,28 and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/24/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/811,772.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on 09/21/2006 regarding application 10/625,631 filed on 07/24/2003 has been entered. Amendment and remarks accompanying applicants' submission have been reviewed. Responses are provided as below. Claims 1 – 13 and Claims 16 – 27 were cancelled. Claim 29 is newly added. Claims 14, 15, 28 and 29 remain pending in the application.

Claim Objections

2. Claims listed below are objected to because of the following informalities:

Claim 14, line 4, before "placement" delete —**the**—.
Claim 15, line 4, change "the environment" to —**an environment**—.
Claim 15, line 4, after "processing" delete —**the**—.
Claim 15, line 5, before "piece" insert —**a**—.
Claim 15, line 8, checking the placement" to —**checking the series of placement**—.
Claim 29, line 2, after "history" insert —**information**—.
Claim 29, line 2, before "program" insert —**placement and wiring processing**—.
Claim 29, line 2 – 3, delete —**of placement and wiring**—.
Claim 29, line 5, checking the placement" to —**checking the series of placement**—.

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 14, 15, 28 and 29 are rejected under 35 U.S.C. 102(b) as being unpatentable over U.S. Patent No. 5,050,091 to *Rubin*.

5. As to Claim 14, *Rubin* shows and discloses the following subject matter:

- A method of *controlling* (i.e., *processing*) connectivity (i.e., wiring) and (polygon) placement of electrical circuits while modifying the design of such circuits – [col. 1, line 17 – 21; col. 2, line 1 – 21];
- *Computer program* (e.g., *placement and wiring processing program*) for controlling the operation of a sequence of synthesis tools – [col. 6, line 40 – 48];
- Reading out a *placement and wiring processing program* from a *mass storage unit* 604 (i.e., *program storage unit*) – [Fig. 6];
- Copying said read out *placement and wiring processing program* on from the *mass storage unit* 604 (*program storage unit*) to *main memory* 606 (i.e., hard drive or RAM – a *storage unit*) to be retrieved by a central processor 607 of a computer – [Fig. 6]; establishing an interactive graphic design system (i.e., *standard hardware design environment*) by using a graphic editor and display monitor 601 – [Fig. 6; col. 1, line 49 – col. 2, line 43]; analysis and synthesis tool in an environment of circuit layout – [abstract]; Notice that the graphic design system is an industrially well-known standard hardware design environment, which executes a program for operating and processing the placement and wiring to design a layout of a piece of an integrated circuit;
- Executing *placement and wiring processing* by a control system 612 based on said placement and wiring processing program stored in the *main memory* 606 (hard drive or RAM – a *storage unit*);
- A programmable logic array (PLA) generator include a *program* (i.e., an executable placement and wiring program) for use (in placement and routing) in generating programmable logic arrays...the (PLA generator) program provides (*functional) commands* guide to placement process and a router to layout a programmable logic array for implementing a desired function – [col. 8, line 24 – 32]; Notice that (1) to change a function of PLA, the (functional) commands in the program (for placement and wiring processing) needs to be modified (2) program storage unit (mass storage 604) and storage (main memory 606) are isolated, and they functioning independently (3) *to modify an executable (placement and wiring) program, some source codes needed to be modified, and modified source codes*

needed to go through compiling and linking to achieve an executable placement and wiring program being implemented by a placement processor and a router. Therefore, the modification needed to be performed on the source codes of the program, which is stored in the program storage unit (mass storage 604).

For reference purposes, the explanations given above in response to Claim 14 are called **[Reference A]** hereinafter.

6. As to Claim 15, *Rubin* shows and discloses the following subject matter:

- A method of *controlling* (i.e., *processing*) connectivity (i.e., wiring) and (polygon) placement of electrical circuits while modifying the design of such circuits – [col. 1, line 17 – 21; col. 2, line 1 – 21];
- *Computer program* (e.g., *placement and wiring processing program*) for controlling the operation of a sequence of synthesis tools – [col. 6, line 40 – 48];
- Reading out a *placement and wiring processing program* from a *mass storage unit* 604 (i.e., *program storage unit*) – [Fig. 6];
- Copying said read out *placement and wiring processing program* on from the *mass storage unit* 604 (*program storage unit*) to *main memory* 606 (i.e., hard drive or RAM – a *storage unit*) to be retrieved by a central processor 607 of a computer – [Fig. 6]; establishing an interactive graphic design system (i.e., *standard hardware design environment*) by using a graphic editor and display monitor 601 – [Fig. 6; col. 1, line 49 – col. 2, line 43]; analysis and synthesis tool in an environment of circuit layout – [abstract]; Notice that the graphic design system is an industrially well-known standard hardware design environment, which executes a program for operating and processing the placement and wiring to design a layout of a piece of an integrated circuit;
- Storing *execution history information* associated with every placement and wiring processing executed by a program (i.e., an *executable placement and wiring processing program*) in a *database 615* – [Fig. 6; col. 4, line 18 – 20, line 39 – 41]; database change means 615 for *updating database 615* – [Fig. 6; col. 6, line 26 – 30]; *Notice that (1) execution history information is stored in database 615 (2) updating database is to store new execution history information*;

- Design rule checker – Checking placement and wiring processing operated through said placement and wiring processing program based on (execution history) information stored in the database 615 – [Fig. 6; col. 6, line 6, line 29 – 30];
- Display system 150 for display *error messages* (i.e., *error information*) detected by design rule checker – [col. 11, line 1 – 11; col. 12, line 16 – 18; col. 9, line 25 – 42].

For reference purposes, the explanations given above in response to Claim 15 are called **[Reference B]** hereinafter.

7. As to Claim 28, reasons are included in **[Reference A]** given above.

8. As to Claim 29, reasons are included in **[Reference B]** given above

Response to Amendment and Remarks

9. Applicants' amendments and remarks filed on 07/21/2006 have been reviewed. Applicants' arguments have been fully considered but they are not persuasive. Claim 29 is newly added. Detailed responses to Applicants' argument are included in the Office Action given above.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Sun James Lin* whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Jack Chiang* can be reached on (571) 272 - 7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

All responses to this Office Action should be mailed to ***Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450*** or faxed to ***571-273-8300***.

Sun James Lin
Primary Examiner
Art Unit 2825
August 4, 2006

SUN JAMES LIN
PRIMARY EXAMINER